CHARACTERISATION OF UNIPOLAR POWER DEVICES TECHNOLOGY

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Summary The quality of momentous technological steps in unipolar power devices manufacturing was examine by means of capacitance and current measurements using a metal-oxide-semiconductor capacitors (MOS-C). From the low- (lf) and high-frequency (hf) capacitance-voltage (*C-V*) curves, the effective defect charge and energy distribution of Si-SiO_2 interface trap density were extracted, respectively. Performing non-steady capacitance-time (*C-t*) and the time domain constant-capacitance (cC-t) as well as deep level transient spectroscopy (DLTS) techniques we have analysed electrically active defects into Si comprising from metal impurities such as Cu, Fe and Au. The physical analysis of relaxation process indicates that generation parameters are mostly influenced by traps at the Si-SiO_2 interface. Moreover, breakdown voltage measurement confirms high quality and homogeneity of thermal oxide. Low density of carrier traps was achieved by intrinsic gettering technique.

1. INTRODUCTION

It is well known that Si surface pre-oxidation treatment and high quality thermal oxide preparation plays crucial role in unipolar technology. From that point of view, great attention has to be paid on the thermal SiO_2 growing with bulk and Si–SiO_2 interface densities of defects as low as possible. Due to downscaling of device dimension, oxide thickness also decreased thereby bulk defects are suppressed, however, one should keep in mind electrically active defects located at the Si–SiO_2 interface that can exacerbate stability and reliability of unipolar device. Moreover, electrical parameters of power device are partially influenced by defects in the subsurface region of Si. Shrinkage of these defects is permanent task in high-quality substrate preparation and creation of defect-free region, so called denude zone (DZ). Capacitance methods are the most suitable diagnostics tool for investigation of such a effects and process optimalisation as well.

In this work we characterised MOS capacitors (MOS-C) using vf and lf *C-V* curves from which we evaluated free carriers concentration $n(x)$, flat-band voltages V_{FB}, effective defect charge Q_{eff} and energy distribution of Si–SiO_2 interface trap density D_{it}, respectively [1].

Electrically active defects in the subsurface region were explored by measuring of generation lifetime τ_g and surface generation velocity S_g using pulsed MOS-C *C-t* technique, furthermore, depth profile of $\tau_g(x)$ was obtained using the time domain constant-capacitance technique (*cC-t*) which is an modification of conventional *C-t* method [2]. Standard Deep Level Transient Spectroscopy (DLTS) have been also employed to our investigation. Breakdown voltage measurement and time-dependent breakdown were used for determination of SiO_2 layer electric strength [3], [4].

2. EXPERIMENT

An n-type, phosphorus doped, <100>-oriented homogeneous silicon wafer with resistivity 2-5 Ωcm and thickness 300 μm was used as a substrate of the MOS-Cs. The gate SiO_2 layer was prepared by thermal oxidation in an atmosphere of dry oxygen at 900°C. The thickness of the SiO_2 layer was about 40 and 28 nm. Al gates were vapour deposited and patterned photolithographically. After manufacturing the MOS structures, the sample was annealed in $N_2 + H_2$ at 460°C for 20 minutes.

The measurements were performed on the MOS-Cs prepared by standard pre-oxidation treatment (BU3) and samples with intrinsic gettering by poly-Si deposition (DEF2).

The MOS-Cs were characterized by capacitance and current methods. High frequency capacitance *C-V* and non-equilibrium capacitance-time *C-t* measurements were performed using the 4280 1 MHz C Meter/C-V Plotter Hewlett-Packard [5]. Quasistatic *C-V* measurements were performed using the Keithley 595 Quasistatic C-V Meter. DLTS measurements were performed using the Polaron DLT Spectrometer 4900. This spectrometer uses a boxcar detection system for acquiring the DLTS output signal. Breakdown measurements were performed using the Keithley 238 High Current Source Measure Unit

3. RESULTS AND DISCUSSION

The flat-band voltage of MOS-C BU3 was calculated from vf *C-V* curve (Fig. 1) as V_{FB}=-0.5 V, that indicates relatively high effective defect charge of N_{eff}=2.6.10^{11} cm^{-2}. *C-t* curve (Fig. 2) of

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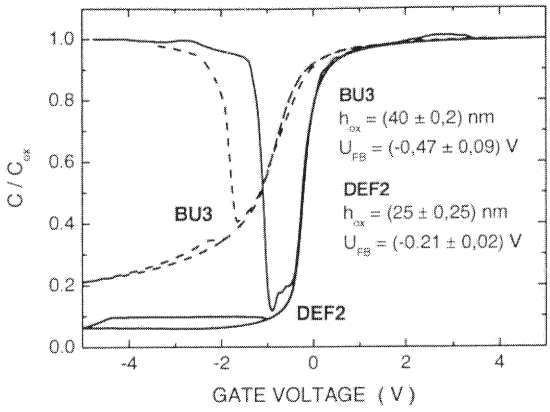

Fig. 1. Lf and hf C-V curves of structures BU3 and DEF2. Oxide thickness and flat-band voltages are also listed.

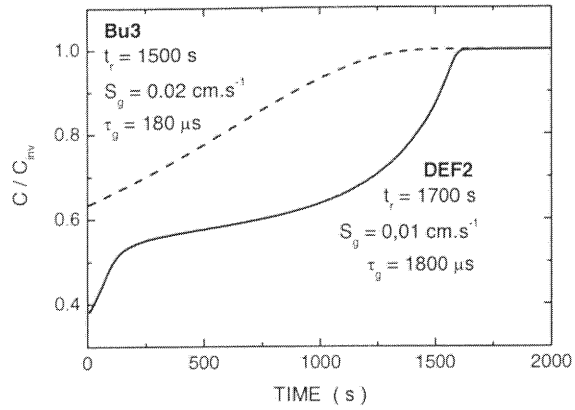

Fig. 2. C-t curves of investigated structures with evaluated generation parameters.

the sample BU3 reveals typical shape with long relaxation process duration (t_r=1500 s). However, there was no marked linear part in the Zerbst plot, therefore extracted lifetime is rather low, while surface velocity is at their typical value. It shows that thermal generation proceeds under non-constant generation rate. We suggest that increasing of generation rate (*i.e.* flow of minority carriers creating inversion layer under gate) is caused by traps located at the Si-SiO_2 interface.

Hence, we investigate Si–SiO_2 interface using quasi-static *C-V* measurement. Interface trap density determined at ±0.1 eV in the Si mid-gap was D_{it}=5,34.10^{14} $m^{-2}eV^{-1}$. According to energy distribution of D_{it} shown in Fig. 3, one can distinguish two deep levels near the mid-gap E_{T1} = E_C-0.52 eV and E_{T2} = E_V+0.49 eV, which can contribute to the enhanced carrier emission, thus generation minority carrier flux. Depth profile of generation lifetime was almost constant through depletion region with value equal to that obtained from Zerbst plot (τ_g=180 μs).

Three deep levels were finding from the DLTS measurement. These levels, also located near the mid-gap, originate from metal impurities of atoms Fe (E_{aFe}=550 meV) and Au (E_{aAu}=540 meV). Third level with activation enthalpy E_{aCu}=530 meV was identified as Cu impurity and we associate this level to the E_{T1} obtained from energy distribution of D_{it}. The cross-section of all the traps was very low (σ=5,5.10^{-19} cm^2), consequently their electrical activity play insignificant role.

The measurement of breakdown voltages revealed typical process of drift current flow, which is given by SiO_2 quality and homogeneity. The value of breakdown voltage (V_{br}≅40 V) does not change with lateral position on the wafer. We did not observe time dependent oxide breakdown.

Regarding to vf *C-V* measurement of MOS-C DEF2 (Fig. 1) it can be seen that positive defect charge is lower according to sample BU3 (V_{FB}=-0.2V a N_{of}=0,91 – 1,8.10^{11} cm^{-2}), whereas *C-t* curve reveals unusual shape. Here, steep increasing of capacitance, thus generation current appear at the earliest part of the relaxation process (up to 200 s). Since the Zerbst model could not be used for such a transient due to non-constant generation kinetics, we can explain the shape of observed *C-t* curve from depth profile of generation lifetime shown in Fig. 4. The *cC-t* technique for depth profiling of generation lifetime measurement represents a modification of *C-t* method under constant depletion width maintaining by controlled voltage ramp. At the Fig. 4, *Hold Time* is the time interval between pulsing the MOS-C into deep depletion and applying controlled voltage ramp, hence, MOS-C followed *C-t* curve at this time interval. When the *Hold Time* is passed, capacitance is kept constant.

Fig. 4 shows creation of DZ in Si depth (up to 3 μm), which is consistent with the earliest part of the *C-t* curve. Generation lifetime then increases toward surface but at approximately 2 μm it again becomes decrease. However, from *cC-t* measurement with *Hold Time*=300 s we find lifetime in order of ms in subsurface region (≈1 μm). So, it can be deduced that decline of generation lifetime at the beginning of depth profile is caused by surface generation while bulk is of high-quality.

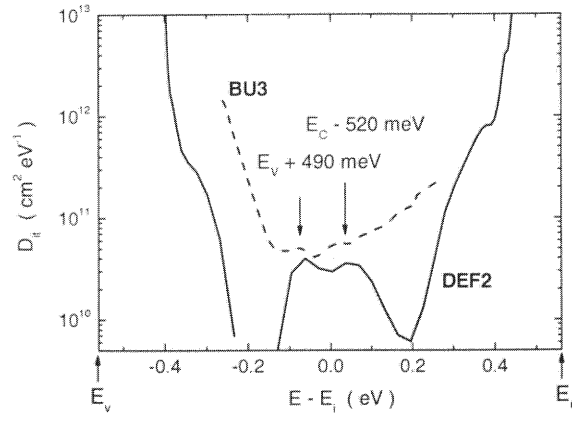

Fig. 3. Energy distribution of interface trap density. Arrows label deep levels from the left side as E_V+0.49 and E_C-0.52 eV, respectively.

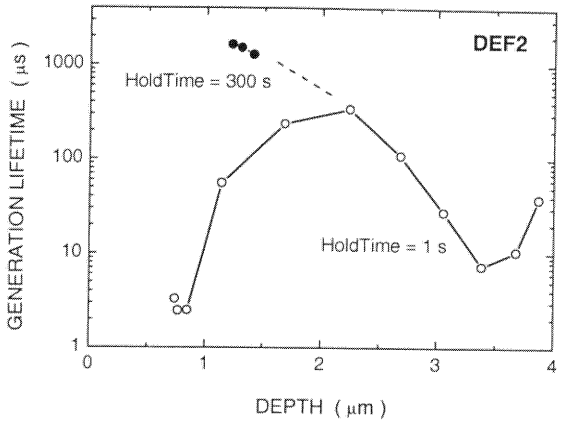

Fig. 4. Depth profile of generation lifetime of the sample DEF2 for Hold Time 1 s (fill circles) and 300 s (open circles). Dash line is drowning for eyes leading only.

In the other words, $\tau_g(x)$ measured with *Hold Time*=300 s is correct without influence of Si-SiO_2 interface trap emission. Our suggestion is supported with $D_{it}(E)$ measurement where, again, two deep levels were identified which can act as efficient generation centres. Note that surface generation is time dependent during relaxation and can control this process if the lifetime is extremely high.

On the contrary, we connect decreasing of lifetime deeper in the bulk (~3.5 μm) with presence of oxide precipitates.

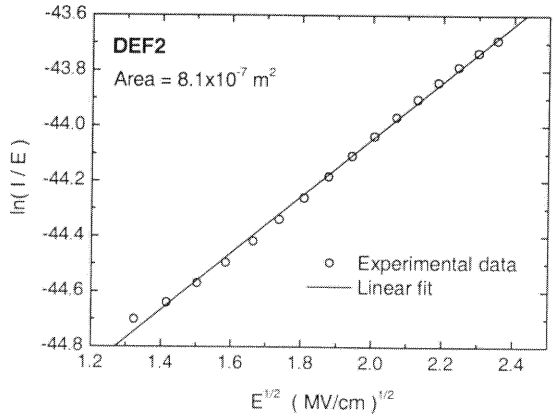

Fig. 6. Poole-Frenkel plot for SiO_2 layer of MOS-C DEF2.

Breakdown measurement reveals elevated conductance of insulator layer due to Poole-Frenkel emission. This effect was clearly demonstrates in the time-dependent breakdown measurement (Fig. 5) and on the plot of $\ln(I/E)$ versus $E^{1/2}$ (Fig. 6) which is commonly used to determine the dominant

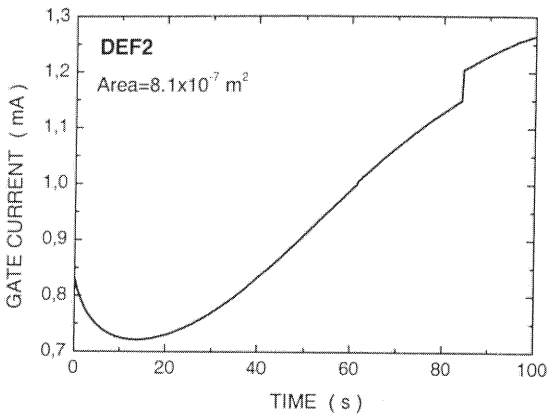

Fig. 5. Time-dependent breakdown of the sample DEF2.

leakage current mechanism. The value of breakdown voltage was V_{br}=38 V.

Two deep levels were detected with activation enthalpies and capture cross-sections E_{a1}=403 meV, E_{a2}=371 meV and σ_1=1,8.10^{-20} cm^2, σ_2=2,5.10^{-20} cm^2, respectively from DLTS measurement. We assume that these levels originate from metal impurities of Ni (E_{aNi}=410 meV) a W (E_{aW}=370 meV).

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